IN THE CLAIMS

Claims 1-9. (canceled)

Claim 10. (currently amended) A MIS transistor comprising ~~including~~:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film;

first side walls being insulative and formed on said silicon substrate on both sides of said gate electrode~~, said first side walls being higher than said gate electrode from said silicon substrate~~;

wherein said gate electrode includes:

a silicon film formed on said gate insulating film, and

a silicide film formed on a surface of said silicon film,

wherein said silicon film has second side walls ~~ON~~ on inner walls of said first side walls,

wherein said silicide film has a plane portion held between said second side walls, and

~~said silicide film has a smaller thickness than a height of~~ wherein said first side walls and said second side walls ~~from~~ are higher than said plane portion.

Claim 11. (original) The MIS transistor in accordance with claim 10, wherein both of said surfaces of said gate electrode and said silicon films are roughened.

Claim 12. (previously presented) A MIS transistor including:

a silicon substrate having a main surface;

a gate electrode being formed to be opposed to said main surface through a gate insulating film and having a silicified portion at an opposite side of said gate insulating film;

side walls being formed on said main surface on both sides of said gate electrode, and having L-shaped sections being higher than said silicified portion; and

impurity regions formed inside said main surface to be opposed to said gate electrode in regard to said side walls, each of said impurity regions having a silicified surface.

Claim 13. (original) The MIS transistor in accordance with claim 12, wherein a surface of said gate electrode is roughened.